

b³

-- BRIEF DESCRIPTION OF THE DRAWINGS --

On page 4, after the third paragraph, add the following:

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-- DETAILED DESCRIPTION OF THE INVENTION --

On page 10, delete the second paragraph containing the words "Figure 8."

In the Claims

Please amend the claims as follows:

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1. (AMENDED) A method of manufacturing an integrated circuit, which method includes a stage wherein lateral isolation regions (spacers) are formed at the sides of a projecting polysilicon region so as to be in contact therewith, said lateral isolation regions each being composed of a smaller isolation layer (402) that is formed by depositing an oxide layer over and around the polysilicon region in a single step, which is in contact with said projecting region (2), and of a larger isolation layer, which method also includes a silicidation process to which the upper part of the polysilicon region is subjected, which silicidation process includes the deposition on said upper part of a metal layer which is capable of forming a metal silicide (5) with the silicon, characterized in that the silicidation process includes, prior to the deposition of said metal layer, an etch step to which at least the vertical portion of the smaller isolation layer (402) is subjected so as to form a trench (TR) between the larger isolation layer (411) of each lateral isolation region and the corresponding side (F) of the polysilicon region (2), wherein the

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trench comprises a depth that is maximally half the height of the larger isolation area, and
in that the deposition of the metal layer is a directional deposition.

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3. (AMENDED) A method as in claim 1, characterized in that the depth (h) of the trench
is equal to maximally half the thickness (E) of the larger isolation layer.

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6. (AMENDED) An integrated circuit comprising lateral isolation regions formed at the
sides of a least one projecting region of polysilicon so as to be in contact therewith, each
lateral isolation region being composed of a smaller isolation layer (402), contacting said
projecting region (2), and a larger isolation layer (411), and comprising a zone (5)
including a metal silicide situated in the upper part of the polysilicon region (2),
characterized in that each lateral isolation region comprises a vertical trench (TR) made
in the smaller isolation layer (402) between the larger isolation layer (411) and the
corresponding side (F) of the projecting region (2), said trench (TR) extending from the
top of the larger isolation layer (411) of the corresponding lateral isolation region down
to a depth (h), and wherein the metal silicide includes a substantially planar surface that is
above the larger isolation layer.

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9. (AMENDED) An integrated circuit as claimed in claim 6, characterized in that each
lateral isolation region comprises a horizontal trench (TH) made in the smaller isolation
layer (402) between a larger isolation layer (411) and the substrate (1) of the integrated
circuit.